

S/N: 10/ 761,613  
Docket : CS03-050  
Reply to the Office Action dated 10/04/2005

Page 5

1

2

**AMENDMENTS TO THE CLAIMS**

This listing of claims will replace all prior versions, and listing, of claims in the application:

6

**Listing of claims:**

8

9

1. (CURRENTLY AMENDED) A method of forming a semiconductor device comprising:

a) forming a gate structure over a substrate being doped with a first conductivity type impurity;

b) performing a doped depletion region implantation by implanting ions being the a second conductive type to into the substrate to form doped depletion regions; ~~beneath and separated from said source/drain regions;~~

c) performing a S/D ~~implantation implant~~ by implanting ions having a the second conductivity type into the substrate to form S/D source and drain regions adjacent to said gate structure; the doped depletion regions are beneath and separated from said source and drain regions;

(1) said doped depletion regions ~~have~~ having an impurity concentration and thickness so that said doped depletion regions are depleted due to a built-in potential created between said doped depletion regions and said substrate.

24

2. (CURRENTLY AMENDED) The method of claim 1 wherein said doped depletion region regions are not formed under said gate structure.

3. (CURRENTLY AMENDED) The method of claim 1 which further includes said doped depletion regions ~~have a~~ having an impurity concentration so that ~~the a~~ built-in

S/N: 10/ 761,613  
Docket : CS03-050  
Reply to the Office Action dated 10/04/2005

Page 6

- 1 junction potential between said doped depletion regions and said substrate forms  
2 depletion regions in the substrate between the ~~source/drain~~ source and drain regions and  
3 the doped depletion ~~regions~~ region;  
4 said depletion regions have a net impurity concentration of the first conductivity  
5 type.  
6
- 7 4. (CURRENTLY AMENDED) The method of claim 1 which further includes said  
8 doped depletion regions ~~have a~~ having an impurity concentration so that ~~the a~~ built-in  
9 junction potential between said doped depletion regions and said substrate forms  
10 depletion regions in the substrate between the ~~source/drain~~ source and drain regions and  
11 the doped depletion region; said depletion regions have a net impurity concentration of  
12 the first conductivity type;  
13 said depletion regions have a net impurity concentration between 1E16 to 5E18  
14 atom/cc.  
15
- 16 5. (CURRENTLY AMENDED) The method of claim 1 which further includes  
17 implanting ions of ~~a the~~ the first impurity type into said substrate between said ~~source/drain~~  
18 source and drain regions and said doped depletion regions.  
19
- 20 6. (CURRENTLY AMENDED) The method of claim 1 which further includes  
21 performing an implant type selected from the group consisting of Halo implant, threshold  
22 voltage implant, and a field implant, that implant ions of ~~a the~~ the first impurity type into  
23 said substrate at least between said ~~source/drain~~ source and drain regions and said doped  
24 depletion regions.  
25
- 26 7. (CURRENTLY AMENDED) The method of claim 1 wherein ~~the a~~ a region of said  
27 substrate between said source/drain regions and said doped depletion regions has a  
28 concentration of ~~a the~~ the first conductivity type impurity between 1E16 to 1E18 atom/cc;  
a channel region in said substrate under said gate structure; said channel region has a  
concentration of a second type impurity between 1E16 to 1E18 atom/cc.

S/N: 10/ 761,613  
Docket : CS03-050  
Reply to the Office Action dated 10/04/2005

Page 7

- 1  
2 8. (CURRENTLY AMENDED) The method of claim 1 wherein said doped depletion  
3 regions are fully depleted.  
4 9. (CURRENTLY AMENDED) The method of claim 1 which further includes performing  
5 LDD implantation by implanting ions being a the second conductivity type into the  
6 substrate using the gate structure as a mask to form LDD regions.  
7 10. (CURRENTLY AMENDED) The method of claim 1 which further includes  
8 performing a LDD implantation by implanting ions being a the second conductivity type  
9 into the substrate using the gate structure as a mask to form LDD regions;  
10 the LDD regions are formed before the doped depletion regions.  
11 11. (CURRENTLY AMENDED) The method of claim 1 which further includes  
12 performing a LDD implantation by implanting ions being a the second conductivity type  
13 into the substrate using the gate structure as a mask to form LDD regions;  
14 wherein the doped depletion regions are formed after the LDD regions.  
15 12. (CURRENTLY AMENDED) The method of claim 1 wherein said first ~~conductive~~  
16 conductivity type is p-type and said substrate has a boron concentration between 1E17  
17 to 1E19 atom/cc.  
18 13. (CURRENTLY AMENDED) The method of claim 1 wherein said first ~~conductive~~  
19 conductivity type is n-type and said substrate-100 has a an As or P concentration  
20 between 1E 17 to 1E 19 atom/cc.  
21 14. (CURRENTLY AMENDED) The method of claim 1 wherein said ~~first conductive~~  
22 type substrate is comprised of Si or SiGe or strained Si, or relaxed SiGe or strained Ge.  
23 15. (ORIGINAL) The method of claim 1 wherein said gate structure has a channel width  
24 between 0.04 and 0.5  $\mu\text{m}$ .  
25  
26 16. (CURRENTLY AMENDED) The method of claim 1 ~~wherein~~ which further includes  
27 performing a LDD implantation by implanting ions being the second conductivity type  
28 into the substrate using the gate structure as a mask to form LDD regions;

S/N: 10/ 761,613  
Docket : CS03-050  
Reply to the Office Action dated 10/04/2005

Page 8

1 the LDD implantation is performed by implanting As ions at a dose between  $5E14$  and  
2  $1E16$  atoms /cm<sup>2</sup>, at an energy between 1keV and 10 keV.

3 17. (CURRENTLY AMENDED) The method of claim 1 ~~wherein which further includes~~  
4 performing a LDD implantation by implanting ions being the second conductivity type  
5 into the substrate using the gate structure as a mask to form LDD regions;

6 the LDD implantation is performed by implanting Boron ions at a dose between  $1E14$   
7 and  $5E15$  atoms /cm<sup>2</sup>, at an energy between 1 keV and 10 keV.

8  
9 18. (CURRENTLY AMENDED) The method of claim 1 wherein the doped depletion  
10 region implantation is performed by implanting As or P ions at a ~~does dose~~ between  
11  $5E12$  and  $5E13$  atoms/cm<sup>2</sup>, at an energy between 100 keV and 500 keV; said doped  
12 depletion region ~~has having~~ a minimum depth below ~~the substrate~~ a surface of said  
13 substrate between 0.09 and 0.7  $\mu$ m.

14 19. (CURRENTLY AMENDED) The method of claim 1 wherein the doped depletion  
15 region implantation is performed by implanting boron ions at a ~~does dose~~ between  $5E11$   
16 and  $5E13$  atoms/cm<sup>2</sup>, at an energy between 50 keV and 200 keV; said doped depletion  
17 region ~~has having~~ a minimum depth below ~~the substrate~~ a surface of the substrate  
18 between 0.09 and 0.7  $\mu$ m.

19 20. (CURRENTLY AMENDED) The method of claim 1 wherein the S/D implantation  
20 implant is performed by implanting arsenic (As) or phosphorus (P) ions at a dose  
21 between  $5E14$  to  $1E16$  atoms/cm<sup>2</sup>, at an energy between 50 keV and 80 keV; said  
22 ~~Source/drain source and drain regions have~~ having a depth below ~~the substrate~~ a surface  
23 of said substrate of between 0.04 and 0.5  $\mu$ m.

24 21. (CURRENTLY AMENDED) The method of claim 1 wherein said second  
25 conductivity type is p-type; and said S/D implant is performed by implanting boron ions  
26 at a dose between  $5E14$  to  $1E16$  atoms/cm<sup>2</sup>, at an energy between 50keV and 80keV; said  
27 ~~source/drain source and drain regions have~~ a depth below the substrate a surface of said  
28 substrate of between 0.04 and 0.5  $\mu$ m.

S/N: 10/ 761,613  
 Docket : CS03-050  
 Reply to the Office Action dated 10/04/2005

Page 9

1 22. (CURRENTLY AMENDED) The method of claim 1 which further includes said gate  
 2 structure having sidewalls; and forming one or more spacers on the sidewalls of said gate  
 3 structure.

4  
 5 23. (CURRENTLY AMENDED) A method of forming a semiconductor device comprising:

- a) forming a gate structure over ~~on~~ a substrate being doped with a first conductivity type impurity;
- b) performing a doped depletion region implantation by implanting ions being ~~the~~ a second ~~conductive~~ conductivity type to the substrate to form doped depletion regions beneath and separated from said source/drain regions;
  - (1) said doped depletion regions have an impurity concentration and thickness so that said doped depletion regions are depleted due to a built-in potential created between said doped depletion regions and said substrate;
  - (2) ~~said doped depletion regions have a impurity concentration so that the built in junction potential between said doped depletion regions and said substrate forms depletion regions in the substrate between the source/drain regions and the doped depletion region; said depletion regions have a net impurity concentration of the first conductivity type; said depletion regions have a net impurity concentration between 1E16 to 1E18 atom/cc;~~
- c) performing a S/D ~~implantation~~ implant by implanting ions ~~having a~~ being the second conductivity type into the substrate to form ~~S/D source and drain~~ source and drain regions adjacent to said gate structure;
  - (1) said substrate between said ~~source/drain~~ source and drain regions and said doped depletion regions has a concentration of a the first type impurity between 1E16 to 1E18 atom/cc[.];  
said doped depletion regions have an impurity concentration so that the built-in potential between said doped depletion regions and said substrate forms depletion

S/N: 10/ 761,613  
Docket : CS03-050  
Reply to the Office Action dated 10/04/2005

Page 10

regions in the substrate between the source and drain regions and the doped depletion region; said depletion regions have a net impurity concentration of the first conductivity type; said depletion regions have a net impurity concentration between 1E16 to 1E18 atom/cc.

24. (CURRENTLY AMENDED) The method of claim 23 wherein said doped depletion regions ~~region~~ are not formed under said gate structure.

25. (CURRENTLY AMENDED) The method of claim 23 wherein ~~the~~ a region of said substrate between said source/drain regions and said doped depletion regions has a concentration of a said first conductivity type impurity between 1E16 to 1E18 atom/cc;  
a channel region in said substrate under said gate structure; said channel region has a concentration of ~~a the~~ the second conductivity type impurity between 1E16 to 1E18 atom/cc.

26.(CURRENTLY AMENDED) The method of claim 23 which further includes; said gate structure has sidewalls; forming one or more spacers on the sidewalls of said gate structure.

27. (CURRENTLY AMENDED) The method of claim 23 which further includes; said gate structure has sidewalls; forming two or more spacers on the sidewalls of said gate structure prior to the doped depletion region implantation.

#### CLAIMS 28 TO 35 (CANCELED)

36.(NEW) The method of claim 1 which further includes said gate structure has sidewalls; forming one or more spacers on the sidewalls of said gate structure.

37. (NEW) The method of claim 1 which further includes said gate structure has sidewalls; forming two or more spacers on the sidewalls of said gate structure prior to the doped depletion region implantation.

38. (New) A method of forming a semiconductor device comprising:

S/N: 10/ 761,613  
Docket : CS03-050  
Reply to the Office Action dated 10/04/2005

Page 11

forming a gate structure over a substrate being doped with a first conductivity type impurity;

performing a doped depletion region implantation by, using said gate structure as an implant mask and implanting ions being of a second conductive type into the substrate to form doped depletion regions;

performing a S/D implantation by implanting ions of the second conductivity type into the substrate to form source and drain regions adjacent to said gate;

the doped depletion regions are beneath and separated from said source and drain regions; said doped depletion regions have an impurity concentration and thickness so that said doped depletion regions are depleted due to a built-in potential created between said doped depletion regions and said substrate.

39. (New) The method of claim 38 which further includes said doped depletion regions having an impurity concentration so that a built-in junction potential between said doped depletion regions and said substrate forms depletion regions in the substrate between the source and drain regions and the doped depletion regions;

said depletion regions have a net impurity concentration of the first conductivity type.

40. (New) The method of claim 38 wherein said doped depletion regions are fully depleted.